

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	0	"200400117749"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/31 14:58
S2	2	"20040117749"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/31 15:06
S3	7	displ\$5 same constrain\$3 same graph\$\$ same layout same layout and (object same orient\$3 same framework)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/31 15:10
S4	2	"6301686".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/31 15:07
S5	2	"6317864".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/31 15:08
S6	2	"6385758".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/31 15:08
S7	2	displ\$5 same constrain\$3 same graph\$\$ same layout same layout and (object same orient\$3 same framework) and (vLSI or IC or PCB)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/31 15:14
S8	11	displ\$5 same (constraint\$3 near3 graph\$3) same layout and (user or designer or operator)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/31 15:30
S9	91	constrain\$3 same graph\$5 same layout and (user or designer or operator) and "716"/\$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/31 15:32
S10	27	constrain\$3 same graph\$5 same layout and (user or designer or operator) and (subgraph\$3 or (group\$3 near3(element or component))) and "716"/\$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/31 15:40

S12	32	constrain\$3 same graph\$4 same layout and ((user or designer or operator) same (delet\$3 or mov\$3 or posit\$5 or plac\$3 or replac\$3 or repositioning))) and (subgraph or (group\$3 near3 (element or component))) and "716"/\$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/01 14:47
S13	46	constrain\$3 same graph\$4 same layout same (delet\$3 or mov\$3 or posit\$5 or plac\$3 or replac\$3 or repositioning) and "716"/\$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/01 07:34
S14	4	constrain\$3 same graph\$4 same layout same (user or designer or operator) same interact\$3 and "716"/\$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/01 09:13
S15	1	constrain\$3 same graph\$4 same subgraph same class\$3 same layout same (user or designer or operator) and "716"/\$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/01 09:13
S16	9	constrain\$3 same graph\$4 same (subgraph or class\$3 or group\$3 or partition\$3 or divid\$3) same layout same (user or designer or operator) and "716"/\$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/01 09:19
S17	1	(constrain\$3 near3 graph\$4 near3 layout) same (subgraph or class\$3 or group\$3 or partition\$3 or divid\$3) same (user or designer or operator) and "716"/\$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/01 09:20
S18	4	constrain\$3 same graph\$4 same layout same framework and "716"/\$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/01 11:16
S19	0	(graph\$4 near3 layoyt near3 constrain\$3) same (subgraph or group\$3) same (class or classification or type) and "716"/\$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/01 11:19
S20	0	(graph\$4 near3 layoyt near3 constrain\$3) same (subgraph or group\$3) and "716"/\$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/01 11:18
S21	0	(graph\$4 near3 layoyt ) same constrain\$3 same (subgraph or group\$3) and "716"/\$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/01 11:18

S22	0	(graph\$4 near3 layoyt ) same constrain\$3 same (subgraph or group\$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/01 11:19
S23	1	(graph\$4 near3 layout near3 constrain\$3) same (subgraph or group\$3) same (class or classification or type) and "716"/\$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/01 11:19
S24	3	(graph\$4 near3 layout near3 constrain\$3) same (subgraph or group\$3) and "716"/\$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/01 11:34
S25	8	(graph\$4 near3 constrain\$3) same layout same (subgraph or group\$3) and "716"/\$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/01 14:39
S28	5	constrain\$3 same (graph\$4 near3 layout) and subgraph and "716"/\$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/01 14:52
S29	9	(constrain\$3 near3 graph\$4) same layout and subgraph and "716"/\$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/01 14:53
S30	14	(constrain\$3 near3 graph\$4) same layout and (graph near3 (classification or classify\$3 or group\$3 or type or position\$3)) and "716"/\$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/01 15:00
S31	14	(constrain\$3 near3 graph\$4) same layout and (graph near3 (classification or classify\$3 or group\$3 or type or position\$3 or sort\$3)) and "716"/\$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/01 15:04
S32	21	constrain\$3 same graph\$4 same layout and (graph near3 (classification or classify\$3 or group\$3 or type or position\$3 or sort\$3)) and "716"/\$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/01 15:05
S33	19	constrain\$3 same graph\$4 same layout and (graph near3 (classification or classify\$3 or group\$3 or type or position\$3 or sort\$3)) and (user or designer or operator) and "716"/\$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/01 15:07

S34	27	constrain\$3 same graph\$5 same layout and (user or designer or operator) and (subgraph\$3 or (group\$3 near3(element or component))) and (delet\$3 or mov\$3 or posit\$5 or plac\$3 or replac\$3 or reposit\$5) and "716"/\$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/01 15:33
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IEEE JNL IEEE Journal or Magazine

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IEEE CNF IEEE Conference Proceeding

IEE CNF IEE Conference Proceeding

IEEE STD IEEE Standard

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- ☐ 1. **Automated hierarchical CMOS analog circuit stack generation intramodule connectivity and matching considerations**  
Naiknaware, R.; Fiez, T.S.;  
Solid-State Circuits, IEEE Journal of  
Volume 34, Issue 3, March 1999 Page(s):304 - 317  
Digital Object Identifier 10.1109/4.748182  
[AbstractPlus](#) | [References](#) | Full Text: [PDF\(2408 KB\)](#) IEEE JNL
- ☐ 2. **Automated Hierarchical Cmos Analog Circuit Stack Generation Intramodule Connectivity and Matching Considerations**  
Naiknaware, R.; Fiez, T.S.;  
Solid-State Circuits, IEEE Journal of  
Volume 34, Issue 3, March 1999 Page(s):304 - 303  
Digital Object Identifier 10.1109/JSSC.1999.748181  
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